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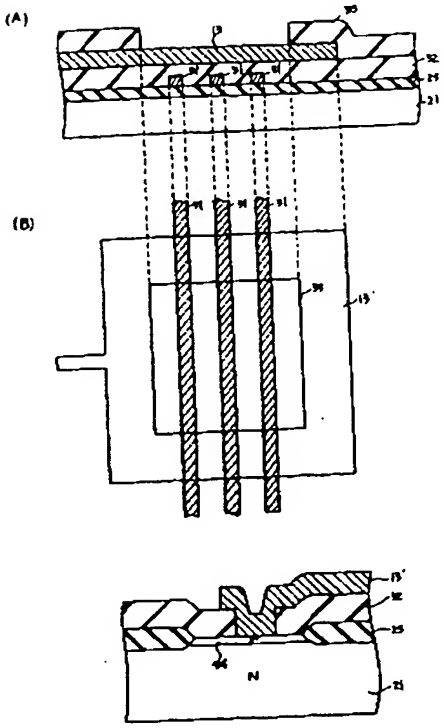
TITLE : SEMICONDUCTOR IC DEVICE



ABSTRACT : PURPOSE: To contrive to reduce the chip area by a method wherein a bonding pad is formed in the field region by the use of the process of multilayer wiring.

CONSTITUTION: The bonding pad 13 is connected to a P^+ type diffused wiring layer 34 formed on an Si substrate 21 via wiring layer 13'. The above-mentioned wiring layer 13' and the bonding pad are formed by patterning of the same Al deposited film. In the formation of such a structure, after Al wiring layers 31 are formed, the process of flattening is performed by deposition of a plasma SiO_2 film 32 over the entire surface. Then, a contact hole to connect the wiring layer 13' to the element part is opened; thereafter an Al film is evaporated over the entire surface and patterned, resulting in the formation of the wiring layer 13' and the bonding pad 13. As a passivation film 33', a PSG film of 1.2μm thickness is deposited over the entire surface, and the part of the bonding pad is opened.

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⑫公開特許公報（A）　昭60－74658

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㊹発明の名称　半導体集積回路装置

㉑特　願　昭58－182773

㉒出　願　昭58(1983)9月30日

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明　細　書

1．発明の名称

半導体集積回路装置

2．特許請求の範囲

回路素子の形成されていないフィールド領域および回路素子の形成されている素子領域が表面に交互に設けられている半導体基板と、該半導体基板を覆って形成された絶縁膜と、該絶縁膜上に形成され、コンタクトホールを介して前記素子領域に形成された回路素子間を接続する配線層と、該配線層を覆って設けられた絶縁膜と、該絶縁膜上に形成され、コンタクトホールを介して前記配線層または前記半導体基板に形成された拡散配線層に接続されて前記フィールド領域上に設けられたボンディングパッドとを具備したことを特徴とする半導体集積回路装置。

3．発明の詳細な説明

（発明の技術分野）

本発明は半導体集積回路装置に関し、特に、ゲートアレイ等のセミカスタムＬＳＩに適したボンディングパッド構造に係る。

（発明の技術的背景）

第１図は、半導体集積回路装置の一例として、従来のゲートアレイを示す平面図である。同図において、１０はゲートアレイチップである。通常、該チップ１０の内部には、回路素子が形成されている素子領域１１…、回路素子が形成されていないフィールド領域１２…が交互に並列して形成されている。そして、チップ１０の内部周縁にはボンディングパッド１３…が形成されている。素子領域１１の具体的な構造は半導体装置の種類によって夫々異なるが、例えば相補型半導体装置（ＣＭＯＳ）の場合には第２図（Ａ）（Ｂ）に示すような構造を有している。同図（Ａ）はパターン平面図であり、そのＢ－Ｂ線に沿う断面図が同図（Ｂ）に示されている。これらの図に於いて、２１はｎ型シリコン基板、２２はｐ型ウエル領域（Ｐ－ウエル）、２３はフィールド酸化膜、２４はゲート酸化膜、２５は多結晶シリコンから成るゲート電極、２６はｎチャンネルＭＯＳトランジ

スタのn⁺型ソースおよびドレイン領域、27はp⁺型ガードリング、28はpチャンネルMOSトランジスタのp⁺型ソースおよびドレイン領域、29はn⁺型ガードリングである。なお、第2図（A）（B）の構造が形成された後、アルミニウム等の配線材料によって適当に配線し、任意の回路が形成される。

他方、第3図（A）（B）は第1図に於けるボンディングパッド13部分を示す拡大図で、同図（A）は断面図、同図（B）はパターン平面図である。図示のように、シリコン基板21表面に形成された厚さ0.8μmの前記フィールド酸化膜23上に、配線層として厚さ0.8μmの第1のアルミニウム層31が形成され、更にその上を覆って厚さ1.4μmのプラズマSiO_2膜32が形成されている。該プラズマSiO_2膜32上には、コンタクトホールを介して前記第1のアルミニウム層31にオーミックコンタクトしたボンディングパッド13が、厚さ1.0μの第2のアルミニウム層をパターンニングすることにより形成

されている。そして、燐珪酸ガラス（PSG）等から成るパッシベーション膜33が全面を覆って形成されており、該パッシベーション膜33に設けられた開孔部によってボンディングパッド13は露出されている。

ところで、第1図の従来のゲートアレイにおいて、通常の場合、素子部11およびフィールド部12の幅L_1、L_2は何れも100～200μmであり、ボンディングパッド13の幅L_3は約100μである。このように、ゲートアレイのようなセミカスタムLSIでは、フィールド領域12の幅L_2が素子領域11の幅L_1と略同じで、他の半導体装置に比較して広くなっている。これはその製造に際して、配線前のDW工程（diffused wafer工程）を総て共通とし、配線工程に於いて任意の回路を構成するため、どの様な配線にも充分に余裕を以て対応できる様にする為である。

（背景技術の問題点）

上述の様に、ゲートアレイを代表とする従来のカスタムLSIはどのような配線に対しても対処

出来なければならない為に、フィールド領域12の幅L_2を広くするのみならず、ボンディングパッド13も余裕をもって実際に用いるよりは数多く形成されている。

この結果、全体のチップ面積が増大せざるを得ないという問題があった。

（発明の目的）

本発明は上記事情に鑑みて為されたもので、セミカスタムLSIの場合に特に問題となる、ボンディングパッド数の増加によるチップ面積の増大を抑制することが可能な半導体集積回路装置を提供するものである。

（発明の概要）

本発明による半導体集積回路装置は、回路素子の形成されていないフィールド領域および回路素子の形成されている素子領域が表層に交互に設けられている半導体基板と、該半導体基板を覆って形成された絶縁膜と、該絶縁膜上に形成され、コンタクトホールを介して前記素子領域に形成された回路素子間を接続する配線層と、該配線層を覆

って設けられた絶縁膜と、該絶縁膜上に形成され、コンタクトホールを介して前記配線層または前記半導体基板に形成された拡散配線層に接続されて前記フィールド領域上に設けられたボンディングパッドとを具備したことを特徴とするものである。

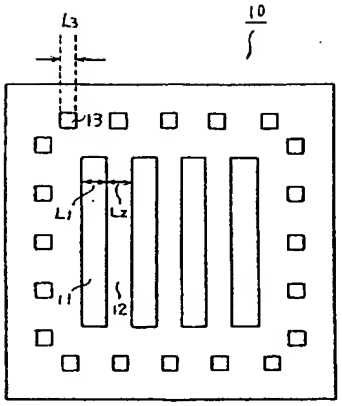
上記本発明によれば、ゲートアレイ等のセミカスタムLSIのフィールド領域が通常の汎用LSIよりも大きいことを利用し、多層配線工程を用いてこのフィールド領域にボンディングパッドを形成することによって、チップ面積の縮小を図ることが出来る。

（発明の実施例）

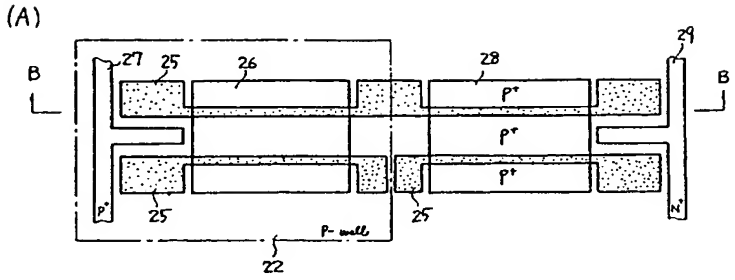
以下、第4図（A）（B）～第図を参照して本発明の一実施例を説明する。

第4図（A）は、本発明の一実施例になるゲートアレイに於いて、そのボンディングパッド部分を示す断面図であり、同図（B）はそのパターン平面図である。これらの図に於いて、第3図（A）（B）と同じ部分には同一の　照　号が付してある。即ち、21はシリコン基板、23はフィール

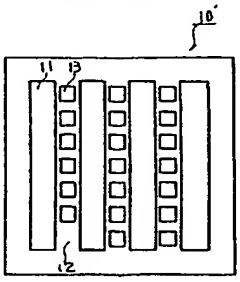
第 1 図

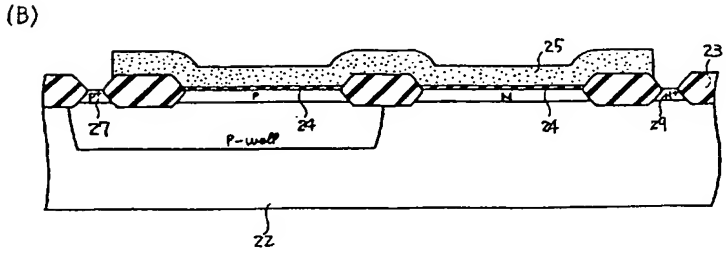


第 2 図

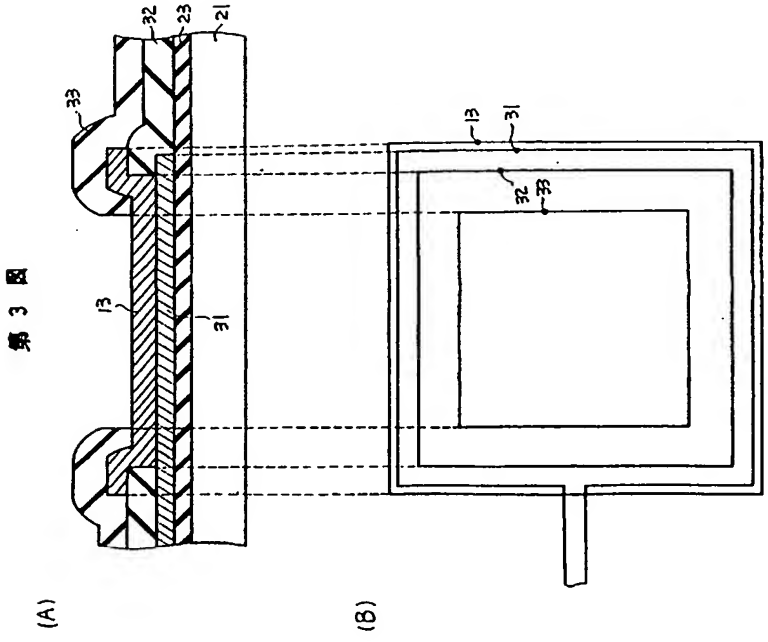


第 6 図





第 3 図



ド酸化膜、３１は第１のアルミニウム配線層、３２はプラズマSiO_2、３３はパッシベーション膜である。ボンディングパッド１３は素子領域間のフィールド領域に形成されている。また、この場合には第１のアルミニウム配線層３１とボンディングパッド１３とは、プラズマSiO_2膜３２により絶縁されている。そして、ボンディングパッド１３は、第５図に示すように、第２のアルミニウム配線層１３´を介してシリコン基板２１に形成されたp^+型拡散配線層３４に接続されている。

なお、第２のアルミニウム配線層１３´とボンディングパッド１３とは同一のアルミニウム蒸着膜をパターンニングして形成されたものである。

上記の構造を形成するに際しては、第１のアルミニウム配線層３１を形成した後、全面にプラズマSiO_2膜３２を堆積し、平坦化加工を行なう。続いて、第６図に示した第２のアルミニウム配線層１３´と素子部とを接続する為のコンタクトホールを開孔した後、全面にアルミニウム膜を蒸着

し、これをパターンニングして第２のアルミニウム配線層１３´とボンディングパッド１３とを形成する。次いで、パッシベーション膜３３´として全面に厚さ１．２μmのＰＳＧ膜を堆積し、ボンディングパッド部分を開孔すれば第４図（Ａ）（Ｂ）および第５図に示す構造が得られる。

上記実施例になるゲートアレイのチップ全体を示せば、第６図の様になる。同図に於いて、１１は素子領域、１２はフィールド領域、１３はボンディングパッドである。図から明らかな様に、この実施例のゲートアレイチップ１０´ではボンディングパッド１３がフィールド領域１２に納められている為、第１図の従来例のようにチップ周縁部にボンディングパッドを形成するための特別の面積を必要としない。従って、チップ１０´の面積は従来に比較して最大で５０％も減少し、大幅に改良された。

（発明の効果）

以上詳述した様に、本発明によればセミカスタムＬＳＩの場合に特に問題となっていた、ボンデ

ィングパッド数の増加によるチップ面積の増大を抑制することが可能な半導体集積回路装置を提供出来るものである。

４．図面の簡単な説明

第１図は従来のゲートアレイを示すチップ平面図、第２図（Ａ）は第１図に於ける素子領域の一部を示すパターン平面図であり、第２図（Ｂ）は同図（Ａ）のＢ－Ｂ線に沿う断面図、第３図（Ａ）は第１図に於けるボンディングパッド部分を拡大して示す断面図であり、第３図（Ｂ）はそのパターン平面図、第４図（Ａ）は本発明の一実施例になるゲートアレイに於いて、そのボンディングパッド部分の構造を示す断面図であり、第４図（Ｂ）はそのパターン平面図、第５図は第４図（Ａ）（Ｂ）の実施例に於けるボンディングパッドと素子部との接続状態を示す断面図、第６図は第１図～第５図の実施例になるゲートアレイのチップ全体を示す平面図である。

１０，１０´…ゲートアレイチップ、１１…素子領域、１２…フィールド領域、１３…ボンディ

ングパッド、１３´…第２のアルミニウム配線層、２１…シリコン基板、２３…フィールド酸化膜、３１…第１のアルミニウム配線層、３２…プラズマSiO_2膜、３３…パッシベーション膜、３４…p^+型拡散配線層

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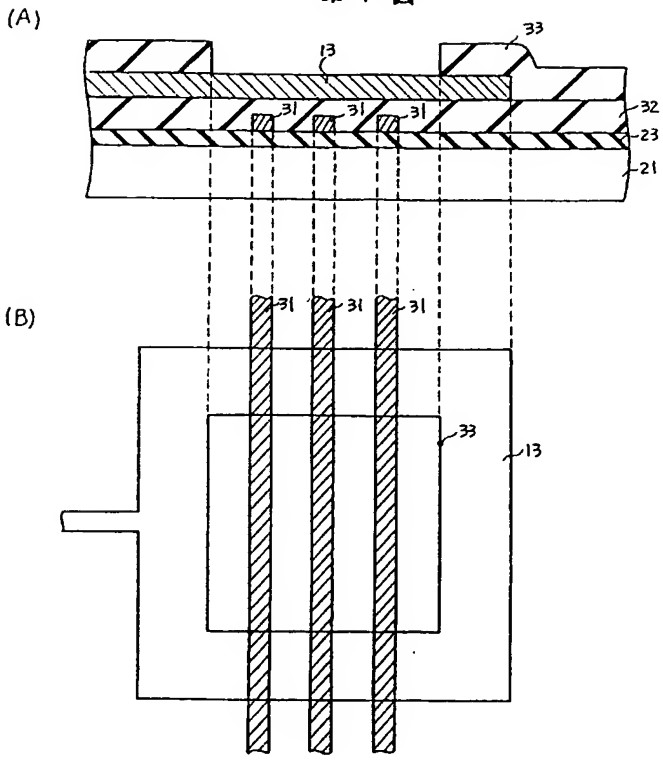
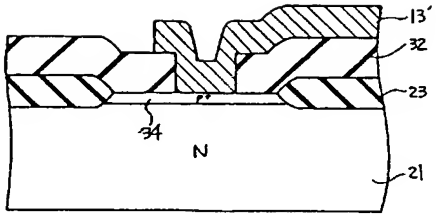
第 4 図



第 5 図



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(54) Semiconductor device in which wiring layer is formed below bonding pad.

(57) In a semiconductor device wherein a bonding pad (22 or 23) is formed on an electrode (17-1 to 17-8, or 18-1 to 18-8) through an insulating interlayer (19) and a bonding wire (25 or 26) is bonded to the bonding pad (22 or 23) by thermocompression bonding, a through hole (21-1 to 21-4, or 20-1 to 20-3) for connecting the bonding pad (23 or 22) and the electrode (17-4 to 17-7, or 18-1 to 18-3) is formed in the insulating interlayer (19) above a contact hole (15-1 to 15-7, or 16-1 to 16-8) for connecting the electrode (17-1 to 17-8, or 18-1 to 18-8) and an active region (13-1 to 13-7, or 12) formed in a semiconductor substrate (11). Metal columns of members of the electrode (17-4 to 17-7, or 18-1 to 18-3) filled in the contact hole (15-4 to 15-7, or 16-1 to 16-3) and members of the bonding pad (23 or 22) filled in the through hole (20-1 to 20-3, or 21-1 to 21-4) are formed under the bonding pad (23 or 22).

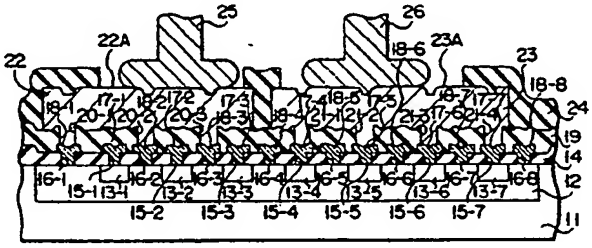

FIG. 1

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Semiconductor device in which wiring layer is formed below bonding pad

The present invention relates to a semiconductor device in which a second wiring metal layer is formed on a first metal wiring layer through an insulating interlayer and wire bonding is performed for the second metal wiring layer and, more particularly, to prevention of cracking of the insulating interlayer formed immediately below a bonding region.

In a conventional bipolar transistor, an emitter region is formed in a comb-like shape in order to reduce an output capacitance, improve high-frequency characteristics, and satisfy a need for increasing an output capacity. The emitter region is formed in a surface part of a base region. The base region is formed in a major surface region of a semiconductor substrate which serves as a collector region. A comb-like emitter electrode is formed on the emitter region so as to correspond to the emitter region. A comb-like base electrode is formed on the base region. The emitter and base electrodes are formed such that teeth of the electrodes are arranged in an interdigital manner at predetermined intervals.

In order to effectively utilize an active region of a transistor, a multilayered structure is utilized in which bonding pads are formed on the emitter and base electrodes through an insulating interlayer. In this case, base and emitter bonding pads are used. The base bonding pad is connected to part of the base electrode through a contact hole formed in the insulating interlayer. The emitter bonding pad is connected to part of the emitter electrode through another contact hole formed in the insulating interlayer. Base and emitter deriving bonding wires are respectively bonded to the bonding pads by thermocompression bonding.

With the above arrangement, the active region can be effectively utilized, and resistances from the emitter and base regions to the corresponding bonding wires can be reduced. In addition, the dynamic characteristics of the transistor can also be improved.

With the above arrangement, however, mechanical stress acts on the insulating interlayer by a pressure during bonding of base and emitter deriving bonding wires. The insulating interlayer is formed on the interdigital base and emitter electrodes, i.e., a portion having a large three-dimensional pattern. Therefore, a three-dimensional portion is formed on the surface of the insulating interlayer accordingly. A bonding pressure tends to be concentrated on a step of the three-dimensional pattern on the surface of the insulating interlayer. For this reason, a crack tends to occur in the insulating interlayer. In the worst case, the insulating interlayer is destroyed. Such a crack cannot be easily found by an initial electrical function test. Therefore, reliability of the semiconductor device is undesirably degraded.

It is, therefore, an object of the present invention to provide a semiconductor device wherein cracking of an insulating interlayer formed immediately under a bonding region can be suppressed, and reliability of the semiconductor device can be improved.

According to an embodiment of the present invention, there is provided a semiconductor device comprising: a semiconductor substrate; an active region formed in a region of a major surface of the semiconductor substrate; a first insulating layer formed on the major surface of the semiconductor substrate which includes the active region; a first contact hole formed at a position in the first insulating layer corresponding to the active region; a first conductive layer formed in the first contact hole and a portion of the first insulating layer around the contact hole; a second insulating layer formed on the first conductive layer and the first insulating layer; a second contact hole formed at a position in the second insulating layer corresponding to the first conductive layer and located above the first contact hole; a second conductive layer formed on the second insulating layer and filled in the second contact hole; and a bonding wire connected to the second conductive layer in regions located above the first and second contact holes.

With the above structure, the pressure applied to the second insulating layer during wire bonding can be supported by columnar portions of the first and second conductive layers filled in the first and second contact holes. Therefore, the pressure acting on the second insulating layer can be reduced to suppress occurrence of cracks, thereby providing a highly reliable semiconductor device.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a sectional view of a semiconductor device according to an embodiment of the present invention; and

Fig. 2 is a plan view showing a pattern of the semiconductor device shown in Fig. 1.

Fig. 1 is a sectional view of a semiconductor device according to an embodiment of the present invention. Fig. 2 is a plan view showing a pattern of the semiconductor device shown in Fig. 1, when taken along the line X - X′ of Fig. 1. Figs. 1 and 2 exemplify an npn bipolar transistor as a semiconductor device having a wiring layer under the bond-

ing pad. N-type semiconductor substrate (silicon substrate 11 serves as a collector region. P-type base region 12 is formed in the major surface region of semiconductor substrate 13. N-type emitter region 13 is formed in a surface region of base region 12. Emitter region 13 has comb-like teeth 13-1 to 13-7. 3,000-Å thick first insulating layer 14 is formed on the major surface of semiconductor substrate 11. Contact hole 15 is formed by photoetching at a position in first insulating layer 14 corresponding to emitter region 13. Contact hole 15 has a shape corresponding to emitter region 13. Contact hole 16 is formed by photoetching at a position in first insulating layer 14 corresponding to base region 12. Contact hole 16 has a shape corresponding to base region 12. Emitter electrode 17 is filled in contact hole 15 and formed on first insulating layer 14 around contact hole 15. Base electrode 18 is filled in contact hole 16 and is formed on first insulating layer 14 around contact hole 16. Emitter and base electrodes 17 and 16 are formed interdigitally. Teeth 17-1 to 17-7 and teeth 18-1 to 18-8 are interdigitally formed at predetermined intervals. Emitter electrode 17 and base electrode 18 are formed such that a 1-μm thick aluminum film or an aluminum alloy film deposited on first insulating layer 14 is patterned by photoetching. Emitter electrode 17 filled in contact hole 15 is brought into ohmic contact with emitter region 13. Base electrode 18 filled in contact hole 16 is brought into ohmic contact with base region 12. 2-μm thick second insulating layer 19 is formed on emitter electrode 17, base electrode 16, and first insulating layer 14. Second insulating layer 19 comprises an insulating interlayer of SiO_2 or Si_3N_4 formed by plasma CVD. Contact holes 20-1 to 20-3 are formed at positions in second insulating layer 19 respectively corresponding to teeth 18-1 to 18-3 of base electrode 18. Contact holes 21-1 to 21-4 are formed at positions in second insulating layer 19 respectively corresponding to teeth 17-4 to 17-7 of emitter electrode 17. Base bonding pad 22 is formed on second insulating layer 19 and filled in contact holes 20-1 to 20-3. Emitter bonding pad 23 is formed on second insulating layer 19 and filled in contact holes 21-1 to 21-4. Bonding pads 22 and 23 are formed such that a 3-μm thick aluminum film or aluminum alloy film is deposited on the second insulating layer and is patterned by photoetching.

Members of base bonding pad 22 filled in contact holes 20-1 to 20-3 are respectively connected to base electrodes 16-1 to 16-3. Members of emitter bonding pad 23 filled in contact holes 21-1 to 21-4 are respectively connected to emitter electrodes 17-4 to 17-7. Passivation film 24 is formed on the resultant structure except for bonding portions 22A and 23A of bonding pads 22 and 23. Base deriving bonding wire 25 is formed on bonding portion 22A by thermocompression bonding. Emitter deriving bonding wire 26 is formed on bonding portion 23A by thermocompression bonding. Ball bonding (this method is also called as nailhead bonding) is performed for bonding bonding wires 25 and 26 by thermocompression bonding. Gold wires are used as bonding wires 25 and 26.

With the above structure, two metal columns are formed under bonding portion 22A. One metal column consists of aluminum of bonding pad 22 filled in contact hole 20-2 and aluminum of base electrode 18-2 filled in contact hole 16-2. The other metal column consists of aluminum of bonding pad 22 filled in contact hole 20-3 and aluminum of base electrode 18-3 filled in contact hole 16-3. These metal columns receive part of the pressure applied to bonding pad 22 during thermocompression bonding of bonding wire 25. Similarly, a metal column is also formed under bonding portion 23A. This metal column consists of aluminum of bonding pad 23 filled in contact hole 21-2 and aluminum of emitter electrode 17-5 filled in contact hole 15-5. The metal column receives part of the pressure acting on bonding pad 23 during thermocompression bonding of bonding wire 26. Therefore, the pressure acting on insulating interlayer 19 can be reduced, and formation of cracks in the step of insulating interlayer 19 can be prevented.

Portions where the metal columns are formed, i.e., the contact portion between bonding pad 22 and teeth 18-1 to 18-3 of base electrode 18 and the contact portion between bonding pad 23 and teeth 17-4 to 17-7 of emitter electrode 17 are preferably formed to cover the entire active region. Then, formation of cracks of insulating interlayer 19 can be suppressed with best efficiency. A wiring resistance from base region 12 to base deriving bonding wire 25 and a wiring resistance from emitter region 13 to emitter deriving bonding wire 26 can also be reduced. However, contact holes may be formed such that the metal columns are formed under only bonding portions 22A and 23A bonded to bonding wires 25 and 26.

The present inventor examined the frequency of occurrence of cracks of the insulating interlayer of the semiconductor device (Figs. 1 and 2) of the present invention and that of the conventional semiconductor device. The materials and thicknesses of base and emitter electrodes, the material and thickness of the first insulating layer, and the material and thickness of the insulating interlayer were identical in the device of the present invention and the conventional device. As a result, the frequency of occurrenc of cracks of the insulating interlayer in the conventional semiconductor device was 60% (12/20 devices), while that of the semi-

conductor device of the present invention was 15% (3·20 devices). As is apparent from this result, the frequency of occurrence of cracks of the insulating interlayer according to the present invention could be confirmed to be greatly reduced as compared with the conventional semiconductor device. When a defective (cracked) semiconductor device was examined with a microscopic picture, cracks in the insulating interlayer were concentrated on the corner portion of the emitter or base electrode pattern. Therefore, these cracks can be assumed to be formed by concentration of stress during bonding.

The above embodiment exemplifies an npn bipolar transistor. However, the present invention is not limited to this type of transistor. The present invention is applicable to a pnp bipolar transistor or any other semiconductor device. In the above embodiment, bonding pads 22 and 23 are formed on insulating interlayer 19. However, the present invention is further applicable to a multilayered wiring structure wherein an insulating interlayer is formed on the first wiring layer and the second wiring layer is formed on the insulating interlayer if the semiconductor device allows bonding of the second wiring layer.

Claims

1. A semiconductor device comprising a semiconductor substrate (11), an active region (12 or 13) formed in a region of a major surface of said semiconductor substrate (11), a first insulating layer (14) formed on said major surface of said semiconductor substrate (11), a first contact hole (15 or 16) formed at a position in said first insulating layer (14) corresponding to said active region (12 or 13), a first conductive layer (17 or 18) formed in said first contact hole (15 or 16) and a portion of said first insulating layer (14) around said contact hole (15 or 16), a second insulating layer (19) formed on said first conductive layer (17 or 18) and said first insulating layer (14), a second contact hole (20-1 to 20-3, or 21-1 to 21-4) formed at a position in said second insulating layer (19) corresponding to said first conductive layer (17 or 18), a second conductive layer (22 or 23) formed on a portion of said second insulating layer (19) and filled in said second contact hole (20-1 to 20-3, or 21-1 to 21-4), and a bonding wire (25 or 26) connected to said second conductive layer (22 or 23),

characterized in that said second contact hole (20-1 to 20-3, or 21-1 to 21-4) is located above said first contact hole (15 or 16), said bonding wire (25 or 26) is bonded on regions of said second conductive layer (22 or 23) at positions above said first and second contact holes (15 or 16; 20-1 to 20-3, or 21-1 to 21-4), and portions of said first conductive layer (17 or 18) filled in said first contact hole (15 or 16) and said second conductive layer (22 or 23) filled in said second contact hole receive part of a pressure which is caused by a pressure applied to said conductive layer (22 or 23) during wire bonding and which acts on said second insulating layer (19).

2. A device according to claim 1, characterized in that said active region includes a first impurity region (12) formed in said region of said major surface of said semiconductor substrate (11) and having a conductivity type opposite to that of said semiconductor substrate (11) and a second impurity region (13) formed in a surface portion of said first impurity region (12) and having the same conductivity type as that of said semiconductor substrate (11).

3. A device according to claim 2, characterized in that said first contact hole (15) is formed in a portion of said first insulating layer (14) on said second impurity region (12), and said first conductive layer (17) is filled in said first contact hole (15) and formed on said first insulating layer (14) around said first contact hole (15).

4. A device according to claim 2, characterized in that said first contact hole (16) is formed in a portion of said first insulating layer (14) on said first impurity region (12), and said first conductive layer (18) is filled in said first contact hole (16) and formed on said first insulating layer (14) around said first contact hole (16).

5. A device according to claim 2, characterized in that said semiconductor substrate (11) serves as a collector region, said first impurity region (12) serves as a base region, and said second impurity region (13) has a comb-like shape and serves as an emitter region.

6. A device according to claim 5, characterized in that said first conductive layer includes a comb-like emitter electrode (17) and a comb-like base electrode (18), said column-like emitter and base electrodes (17, 18) being arranged such that teeth (17-1 to 17-7) of said emitter electrode (17) and teeth (18-1 to 18-8) of said base electrode (18) are interdigitally arranged at predetermined intervals.

7. A device according to claim 1, characterized in that said second insulating layer includes an insulating interlayer (19).

8. A device according to claim 1, characterized in that said second conductive layer includes a bonding pad (22 or 23).

9. A device according to claim 8, characterized in that said bonding wire (25 or 26) is bonded to said bonding pad (22 or 23) by thermocompression bonding.

10. A semiconductor device including a second wiring layer formed on a first wiring layer through an insulating layer and a bonding wire formed on

said second wiring layer, characterized by comprising a semiconductor region (11 or 12) of a first conductivity type, an impurity region (12 or 13) formed in a major surface portion of said semiconductor region (11 or 12) and having a second conductivity type, a first insulating layer (14) formed on said semiconductor region (11 or 12), a first contact hole (12 or 13) formed at a position in said first insulating layer (14) corresponding to said impurity region (12 or 13) of the second conductivity type, a first wiring layer (17 or 18) filled in said first contact hole (15 or 16) and formed on said first insulating layer (14) around said first contact hole (15 or 16), a second insulating layer (19) formed on said first wiring layer (17 or 18) and said first insulating layer (14), a second contact hole (20-1 to 20-3, or 21-1 to 21-4) formed at a position in said second insulating layer (19) corresponding to said first wiring layer (17 or 18), a second wiring layer (22 or 23) filled in said second contact hole (20-1 to 20-3, or 21-1 to 21-4) and formed on said second insulating layer (19), and a bonding wire connected to said second wiring layer (22 or 23),

wherein portions of said first wiring layer (17 or 18) filled in said first contact hole (15 or 16) and said second wiring layer (22 or 23) filled in said second contact hole (20-1 to 20-3, or 21-1 to 21-4) receive a pressure which is caused by a pressure applied to said second wiring layer (22 or 23) during bonding of said bonding wire (25 or 26) to said second wiring layer (22 or 23) and which acts on said second insulating layer (19).

11. A device according to claim 10, characterized in that said first conductive layer includes a comb-like emitter electrode (17) and a comb-like base electrode (18), said column-like emitter and base electrodes (17, 18) being arranged such that teeth (17-1 to 17-7) of said emitter electrode (17) and teeth (18-1 to 18-8) of said base electrode (18) are interdigitally arranged at predetermined intervals.

12. A device according to claim 10, characterized in that said second insulating layer includes an insulating interlayer (19).

13. A device according to claim 10, characterized in that said second conductive layer includes a bonding pad (22 or 23).

14. A device according to claim 13, characterized in that said bonding wire (25 or 26) is bonded to said bonding pad (22 or 23) by thermocompression bonding.

15. A semiconductor device including a bonding pad formed on an electrode through an insulating layer, characterized by comprising a semiconductor substrate (11) of a first conductivity type, a first impurity region (12) formed in a major surface portion of said semiconductor substrate (11) and having a second conductivity type, a comb-like second impurity region (13) formed in a surface layer of said first impurity region (12) and having the first conductivity type, a first insulating layer (14) formed on said semiconductor substrate (11), a first contact hole (15) formed at a position in said first insulating layer (14) corresponding to said second impurity region (13), a second contact hole (16) formed at a position in said first insulating layer (14) corresponding to said first impurity region (12), a comb-like first electrode (17) filled in said first contact hole (15) and formed on said first insulating layer (14) around said first contact hole (15), a comb-like second electrode (18) filled in said second contact hole (16) and formed on said first insulating layer (14) around said second contact hole (16), a second insulating layer (19) formed on said first and second electrodes (17 and 18) and said first insulating layer (14), a third contact hole (21-1 to 21-4) formed at a position in said second insulating layer (19) partially corresponding to said first electrode (17), a fourth contact hole (20-1 to 20-3) formed at a position in said second insulating layer (19) partially corresponding to said second electrode (18), a first bonding pad (23) filled in said third contact hole (21-1 to 21-4) and formed on a portion of said second insulating layer (19), a second bonding pad (22) filled in said fourth contact hole (20-1 to 20-3) and formed on a portion of said second insulating layer (19), a first bonding wire (26) connected to said first bonding pad (23), and a second bonding wire (25) connected to said second bonding pad (22),

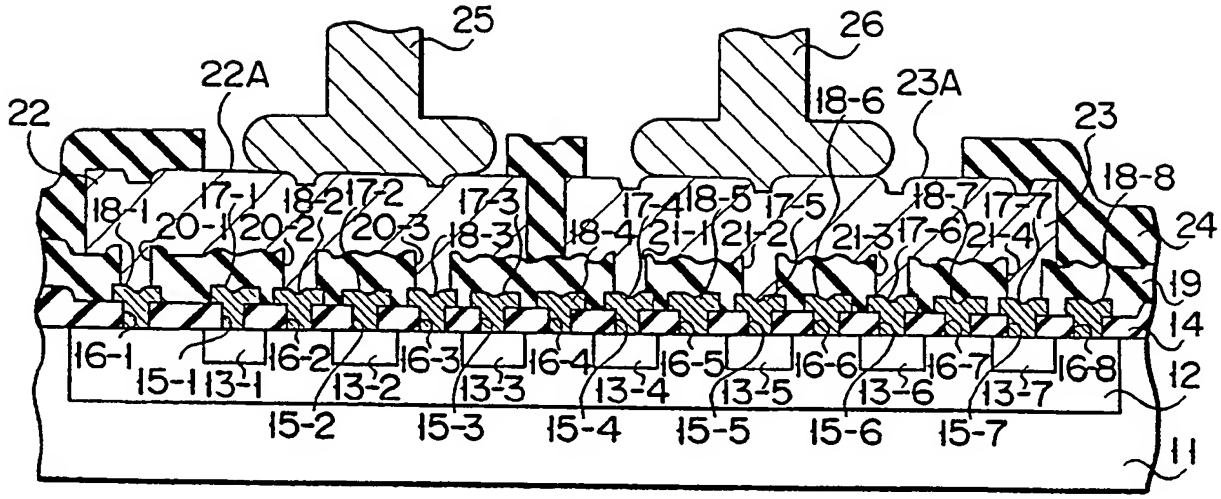
wherein a first portions of a member of said first electrode (17) filled in said first contact hole (16) and a member of said first bonding pad (23) filled in said third contact hole (21-1 to 21-4) receive part of a pressure which is caused by a pressure applied to said first bonding pad (23) during bonding of said first bonding wire (26) to said bonding pad (23) and which acts on said second insulating layer (19), and second portions of members of said second electrode (16) filled in said second contact hole (15) and members of said second bonding pad (22) filled in said fourth contact hole (20-1 to 20-3) receive part of a pressure which is caused by a pressure applied to said second bonding pad (22) during bonding of said second bonding wire (25) to said first bonding pad (22) and which acts on said second insulating layer (19).

16. A device according to claim 15, characterized in that said first electrode includes an emitter electrode (17).

17. A device according to claim 15, characterized in that said second electrode includes a base electrode (18).

18. A device according to claim 15, characterized in that said second insulating layer includes an insulating interlayer (19).

19. A device according to claim 15, characterized in that said first and second bonding wires (25 and 26) are respectively bonded to said first and second bonding pads (22 and 23) by thermocompression bonding.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26
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23A
22
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18-7
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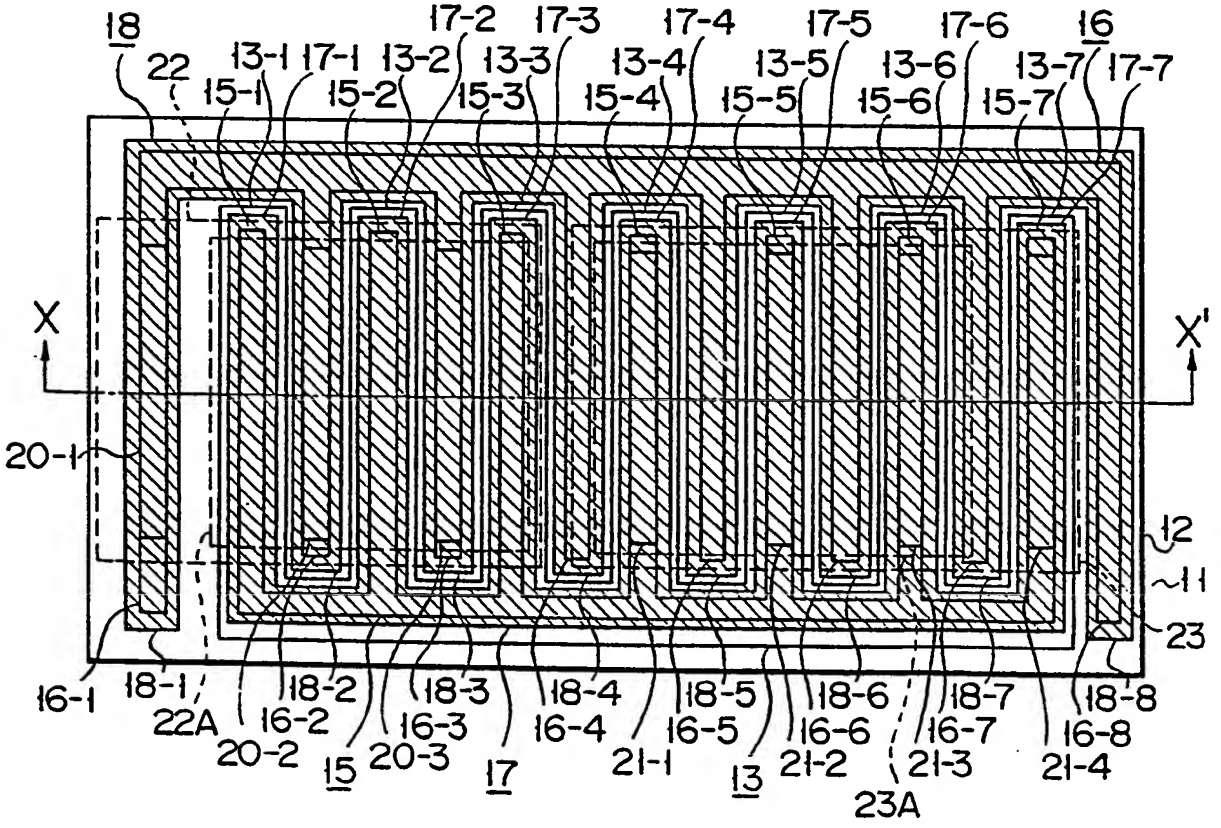
15-6
15-7
11

FIG. 1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16-3
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18-5
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23A
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18-8
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21-4

FIG. 2

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(54) **Semiconductor device in which wiring layer is formed below bonding pad.**

(57) In a semiconductor device wherein a bonding pad (22 or 23) is formed on an electrode (17-1 to 17-8, or 18-1 to 18-8) through an insulating interlayer (19) and a bonding wire (25 or 26) is bonded to the bonding pad (22 or 23) by thermocompression bonding, a through hole (21-1 to 21-4, or 20-1 to 20-3) for connecting the bonding pad (23 or 22) and the electrode (17-4 to 17-7, or 18-1 to 18-3) is formed in the insulating interlayer (19) above a contact hole (15-1 to 15-7, or 16-1 to 16-8) for connecting the electrode (17-1 to 17-8, or 18-1 to 18-8) and an active region (13-1 to 13-7, or 12) formed in a semiconductor substrate (11). Metal columns of members of the electrode (17-4 to 17-7, or 18-1 to 18-3) filled in the contact hole (15-4 to 15-7, or 16-1 to 16-3) and members of the bonding pad (23 or 22) filled in the through hole (20-1 to 20-3, or 21-1 to 21-4) are formed under the bonding pad (23 or 22).

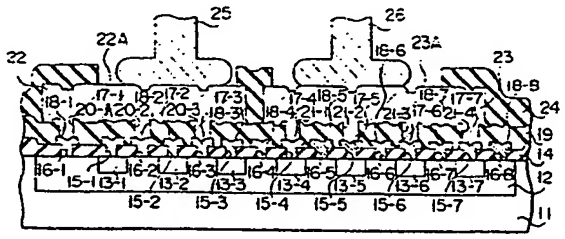

FIG. 1

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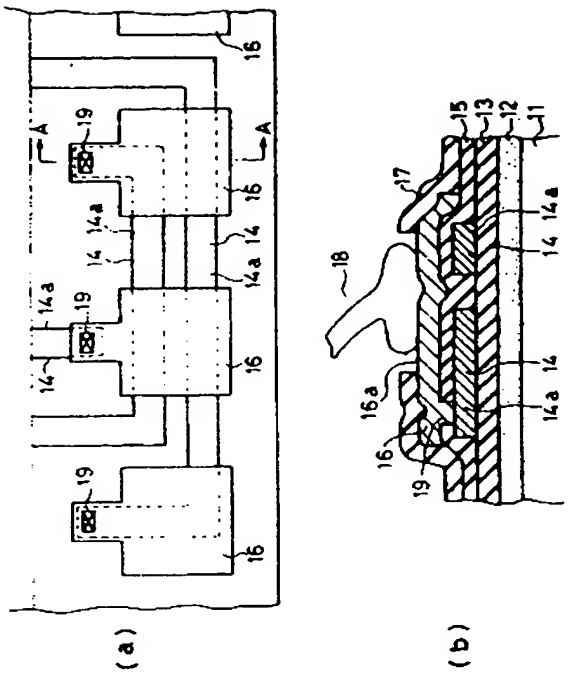
TITLE : SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE



ABSTRACT : PURPOSE: To increase the connection with an internal circuit without increasing chip size and power lines by forming a bonding pad using the uppermost wiring layer, and arranging signal wirings made of lower wiring layer through an insulating layer on the region under the pad.

CONSTITUTION: A field insulating film 12, the first interlayer insulating film 13, the first Al wiring layer (signal wirings) 14, the second interlayer insulating film (insulating layer) 15, the second Al wiring layer 16, the third insulating film 17 as the uppermost insulating layer, a bonding wire 18 and a connecting hole 19 are formed on a semiconductor substrate 11. The layer 16 is partly formed with bonding pad 16a, and connected through a connecting hole 19 to the layer 14. The layer 14 is a connecting wirings 14a, and connected through the lower region of the pad 16a to the input/output circuit of the internal circuit. The layer 15 prevent the disconnection due to the impact at the bonding time.

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 88 10 7501

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	EP-A-0 100 100 (K.K. TOSHIBA) * Abstract; page 4, lines 1-31; claim 1; figure 2 * ---	1,2,8-10,13-17,19	H 01 L 23/48
A	IEDM INTERNATIONAL ELECTRON DEVICES MEETING, 7th-9th December 1981, pages 62-65, IEEE, Washington, D.C., US; K. MUKAI et al.: "A new integration technology that enables forming bonding pads on active areas" * Page 62, "Abstract"; pages 62-63, "Film strength"; figure 2 * -----	1,8-10, 13-15, 19	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

H 01 L 23/00
H 01 L 21/00

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	19-04-1989	DELPORTE B.P.M.

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